AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. – 7. (Canceled)

8. (New)   A nonvolatile semiconductor memory device, comprising:

a memory cell, including a source layer formed in a semiconductor substrate, a drain layer formed in said semiconductor substrate and apart from said source layer, a floating gate formed above a portion of said semiconductor substrate between said source layer and said drain layer, and a control gate formed above said floating gate;

a word line control circuit to drive a word line connected to said control gate;

a program data holding circuit to hold program data;

a programming voltage generator circuit to apply a programming voltage to a bit line connected to said drain layer; and

a discrimination circuit to verify said program data,

wherein programming of said programming data to said memory cell is conducted by injecting hot electrons generated between said source layer and said drain layer into said floating gate, and

wherein verification of said programmed data is conducted by the following steps:

(a)   charging a pre-charge voltage to said bit line;

(b)   making said bit line a floating state, after step (a);

(c)   applying a verify voltage to said word line, after the step (b); and

(d)   discriminating whether said pre-charge voltage is retained or not, depending upon a height of a threshold voltage of said memory cell, after step (c).

9. (New)   The nonvolatile semiconductor memory device, according to claim 8, wherein said discrimination circuit has a verify circuit of a flip-flop type, an insulated-gate type transistor provided between an output node of said verify circuit and said bit line for connecting therebetween, and a circuit formed with a plural number of insulated gate-type transistor groups to convert data verified by said verify circuit, so as to transfer said data to said bit line, wherein the verified data is inverted at least one time in a series of operations of said programming and verification.

10. (New)   A nonvolatile semiconductor memory device, according to claim 8, wherein said semiconductor source layer and said drain layer are each formed of a diffusion layer.